IN THE CLAIMS

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (Original) A computer system comprising:

an operating system;

a first component that comprises a first test module;

a second component that comprises a second test module; and

an interconnect coupling the first component and the second component;

wherein the first test module is configured to provide a first test pattern to the second test module on the interconnect in response to a first signal from the operating system.

2. (Original) The computer system of claim 1 wherein the second test module is configured to detect an error on the interconnect in response to receiving the first test pattern.

3. (Original) The computer system of claim 1 wherein the second test module is configured to provide a second test pattern to the first test module.

4. (Original) The computer system of claim 3 wherein the first test module is configured to detect an error on the interconnect in response to receiving the second test pattern.

5. (Original) The computer system of claim 1 wherein the operating system is configured to provide the first signal to the first test module in response to detecting a second signal from the first test module.

6. (Original) The computer system of claim 5 further comprising:

a processor configured to cause the operating system to be booted;

wherein the first test module is configured to generate the second signal subsequent to the operating system being booted.

7. (Original) The computer system of claim 1 wherein the first component comprises a processor, and wherein the second component comprises a controller coupled to the processor.

8. (Original) The computer system of claim 7 wherein the controller comprises a system controller.

9. (Original) The computer system of claim 7 wherein the controller comprises a memory controller.

10. (Original) The computer system of claim 7 wherein the first test module is configured to provide a second signal to the operating system to cause the processor to be de-allocated from use by the operating system, and wherein the operating system is configured to provide the second signal to the first test module in response to causing the processor to be de-allocated.

11. (Original) The computer system of claim 1 wherein the first component comprises an input / output (I/O) controller, and wherein the second component comprises an input / output (I/O) device coupled to the I/O controller through an expansion slot.

12. (Original) The computer system of claim 11 wherein the first test module is configured to provide a second signal to the operating system to cause the expansion slot to be de-allocated from use by the operating system, and wherein the operating system is configured to provide the second signal to the first test module in response to causing the expansion slot to be de-allocated.

13. (Original) A method performed by an interconnect test module in a computer system comprising:

causing a component coupled to an interconnect to be de-allocated from use by an operating system;

performing a test on the interconnect; and

notifying the operating system in response to detecting an error in performing the test.

14. (Original) The method of claim 13 further comprising:

causing the component to be re-allocated to use by the operating system subsequent to performing the test.

15. (Original) The method of claim 13 further comprising:

reporting results of the test to the operating system.

16. (Original) The method of claim 13 further comprising:

performing the test on the interconnect by providing test patterns on the interconnect.

17. (Original) A system comprising:

a processor configured to cause an operating system to be booted;

an interconnect;

a first test unit coupled to the interconnect; and

a second test unit coupled to the interconnect;

wherein the first test unit is configured to provide a test pattern to the second test unit subsequent to the processor booting the operating system, and wherein the second test unit is configured to detect an error in the interconnect in response to receiving the test pattern.

18. (Original) The system of claim 17 further comprising:

a first switching mechanism coupled to the first test unit; and

a second switching mechanism coupled to the second test unit;

wherein the first test unit is configured to cause the first switching mechanism to connect the first test unit to the interconnect, and wherein the second test unit is configured to cause the second switching mechanism to connect the second test unit to the interconnect.

19. (Original) The system of claim 18 further comprising:

a first component coupled to the first switching mechanism; and

a second component coupled to the second switching mechanism;

wherein the first test unit is configured to cause the first switching mechanism to disconnect the first component from the interconnect, and wherein the second test unit is configured to cause the second switching mechanism to disconnect the second component from the interconnect.

20. (Original) The system of claim 19 further comprising:

a first error log configured to be written by the first test unit; and

a second error log configured to be written by the second test unit.